

## QUAD FLAT NO-LEAD (QFN) FINE PITCH PACKAGING DESIGN AND MANUFACTURING CHALLENGES

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### ABSTRACT

Moving to a fine pitch IC package technology always involves challenges in design and manufacturing. For QFN (Quad Flat No-lead) package, challenges could range from constraints on lead frame design, isolations and proper clearances, considerations on lead frame stability up to board level reliability (BLR).

This paper discusses the challenges encountered in the development of a new 0.35mm pitch QFN package. In order to get to the 0.35mm lead pitch, the lead width needs to be reduced but this can result in some wire bonding problems like NSOL (non-stick on lead) especially on the corner leads. And also a reduced lead width poses risk to board level reliability (BLR) performance. So a combination of design, virtual prototyping or modeling and wire bonding process optimization was used in this study to overcome the challenges in the successful design and manufacturing of a 0.35mm fine pitch QFN package.

### 1.0 INTRODUCTION

QFN (Quad Flat No-lead) package is still being widely used in the semiconductor industries worldwide. But in order to meet the customer demand for smaller packages with increased functionality, there is a need to design finer lead pitch package.

In this paper, developing a new 0.35mm lead pitch QFN package is considered. The schematic of a typical QFN package design is illustrated in Figure 1, which also shows the printed circuit board (PCB). The package is composed of an IC silicon die, which is electrically connected to the package lead by wire bonding. The most widely used wire material is gold (Au). There is typically a first bonding position where a first wire bond is made and a second bonding position where a second wire bond is made. The assembled package is usually soldered to the PCB using SAC (Sn-Ag-Cu) solder paste, a popular lead-free replacement for eutectic solders (Sn-Pb).

The fine pitch package design involves reducing the lead width in order to maintain enough clearance between leads and meet the 0.35mm pitch requirement. However, initial

evaluations showed that there was difficulty in creating a successful wire bond especially on the corner leads. And besides the wire bonding concern, there was also concern on the BLR performance when soldered to the PCB because of the reduced lead width.

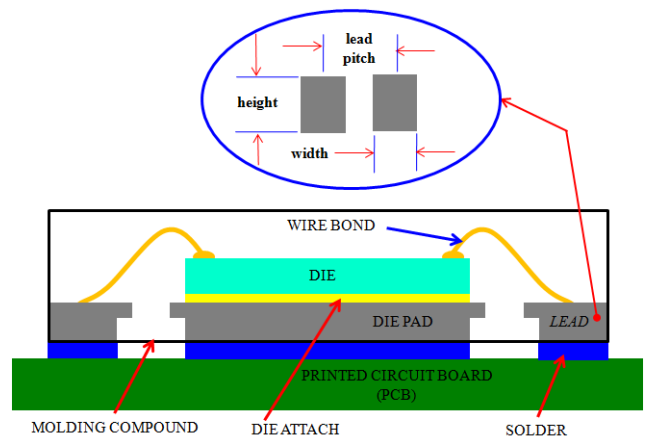


Figure 1. Schematic of a QFN Package soldered to the PCB.

So with the issues encountered in 0.35mm lead pitch wire bonding like NSOL (non-stick on lead), using different wire bonding techniques and wire bond parameter optimization were explored. And since doing an actual BLR test by thermal cycling is costly and tight time-to-market schedule must be met, an established virtual prototyping or modeling method was also used to assess the BLR performance or solder cycle life.

### 2.0 REVIEW OF RELATED LITERATURE

#### 2.1 Wire Bonding Techniques

##### 2.1.1 Forward Bonding

The forward bonding technique<sup>6,7</sup> illustrated in Figure 2 is the conventional method of wire bonding. In this method, the capillary is first located over a first bonding position. A clamp controlling the wire opens and wire extends out of the

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capillary. An electronic flame-off (EFO) spark is generated to create a free air ball at a tail of the wire and the capillary moves towards the first bonding position with the free air ball. The free air ball is placed onto the first bonding position, and ultrasonic energy and pressure is applied onto the ball to create a first wire bond between the wire and the connection pad at the first bonding position.

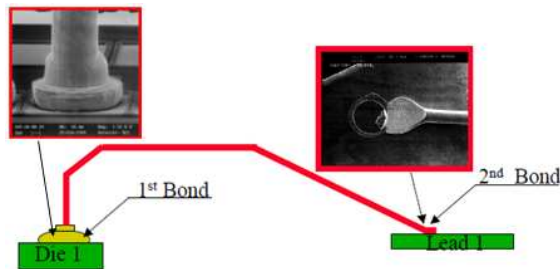


Figure 2. Forward Bonding Technique.

After the first bond is made, the capillary moves away from the first bonding position and wire is extended by the capillary as the capillary is moved towards the second bonding position in order to form a wire loop. The capillary moves to the second bonding position and presses the wire onto second bonding position. Ultrasonic energy and pressure is applied onto the wire and stitch bonding is performed to the wire at the capillary tip, thereby stitching the wire to the connection pad at the second bonding position. After the second bond is made, the capillary moves away from the connection pad at which point the wire has been bonded between two points. As the capillary moves away from the second bonding position, the clamp is closed such that the wire is pulled and severed from the wire bond made at the second bonding position. The second bonding position is normally on the lead finger.

### 2.1.2 Bond Stitch on Ball (BSOB)

BSOB (Bond Stitch on Ball) is used on devices that require die-die wire bonding in multi chip modules (MCM), stacked die and System in Package (SiP) applications. BSOB is also widely used while performing reverse bonding<sup>8</sup>.

In the Bond Stitch on Ball (BSOB)<sup>6,7,9</sup> bonding approach, bump formation was placed on lead finger in preparation for stable 2<sup>nd</sup> bond formation where the 2<sup>nd</sup> bond's wedge will land on top of the stand-off ball.

During gold ball wire bonding, a gold ball is first formed by melting the end of the wire which is held by a bonding tool known as a capillary through electronic flame-off (EFO). Free air ball size consistency is controlled by the EFO and the tail length is critical in good bonding formation.

The free-air ball (FAB) is then brought into contact with the lead finger forming a ball known as bump formation. Adequate amounts of pressure, heat, and ultrasonic forces are then applied to the ball for a specific amount of time, forming the initial metallurgical weld between the ball and the lead finger as well as deforming the ball bond itself into its final shape (Figure 3). Capillary raises and tears the wire as bond head ascend to fire level. EFO fires to form free air ball. Cycle repeats until all stand-off balls are placed.



Figure 3. Stand-off Ball/ Bump

After placing stand-off balls the machine continue to bond wires where 2<sup>nd</sup> bond's wedge will land on top of stand-off ball (Figure 4).

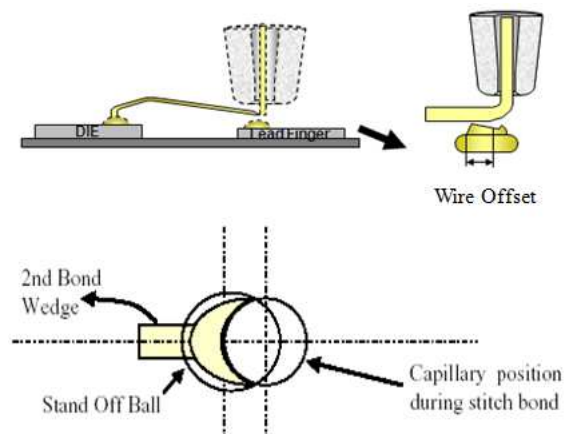


Figure 4. Forming the 2<sup>nd</sup> Bond on Ball/Bump for BSOB.

### 2.2 BLR Modeling and Simulation

In modeling BLR (board level reliability) or predicting solder life, there are different solder constitutive models commonly used in the microelectronics industry. One previous study<sup>1</sup> implemented four different models including elastic-plastic (EP), elastic-creep (Creep), elastic-plastic-creep (EPC) and viscoplastic Anand's (Anand) models in FEA modeling and simulation to investigate solder constitutive model effect on solder fatigue life and stress-strain response. Based on fatigue life prediction, it was shown that Creep, EPC and Anand models are suitable for thermal cycling simulations.

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However, for SAC solders (e.g. SAC 305, SAC405, and SAC387), the hyperbolic sine creep equation is commonly used to model the solder's temperature and time-dependent creep behavior. It is defined as<sup>1,2</sup>:

$$\dot{\epsilon}_c = C_1 \frac{G}{T} \left[ \sinh \left( \alpha \frac{\sigma}{G} \right) \right]^n \exp \left[ \frac{-Q}{kT} \right]$$

When using ANSYS FEA software in doing the analysis, the creep strain rate is simplified and rewritten as:

$$\dot{\epsilon}_c = C_1 [\sinh(C_2 \sigma)]^{C_3} \exp \left[ \frac{-C_4}{T} \right]$$

Table 1 gives the input for ANSYS hyperbolic sine creep model used in this study.

Table 1. Constants for Sn-3.8Ag-0.7Cu Solder<sup>2</sup>

C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>
3.2e4	0.037	5.1	6524.7

The fatigue life prediction could either be based on strain or strain energy. However, Che et al<sup>3</sup> showed that the energy-based fatigue model resulted in accurate and reasonable fatigue life prediction compared to strain-based fatigue model. And in order to reduce the stress concentration effect, the volume-averaging method is typically used in parameter extraction from simulation results for solder fatigue life prediction<sup>4</sup>:

$$W_{cr} = \Sigma(W_{cri} V_i) / \Sigma V_i$$

Once the accumulated strain energy density per cycle ( $W_{cr}$ ) is obtained from the model, the characteristic life can be calculated by the following correlation for SnAgCu(SAC) solders<sup>5</sup>:

$$N_f = 345 W_{cr}^{(-1.02)}$$

### 3.0 EXPERIMENTAL SECTION

#### 3.1 Wire Bond Evaluation

The CMOS die pad technology was used during the evaluation. It is composed of six metal layers for the bond pad and the last metal layer was TiTiN/AlCu/TiN/Arc with 3.093 in thickness. The bond pad opening is 60 microns and bond pad pitch is 70 microns.

Figure 5 shows the design details of the QFN package being evaluated. It has 44 leads and the lead frame finish is NiPdAu with 0.35 mm lead pitch. The die is seated on the leads except the 8 corner leads. The die pad is to be connected to the lead using gold bond wire with a size of 20 microns.

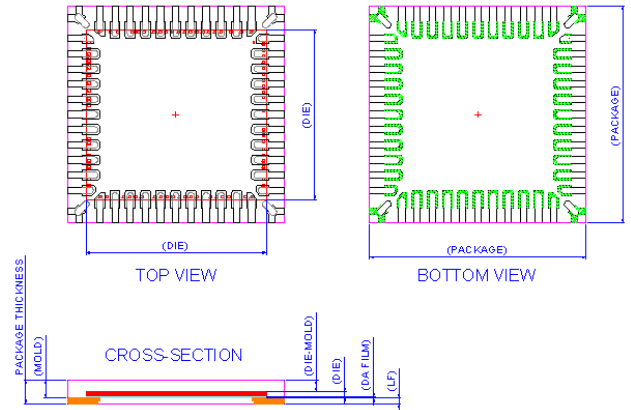


Figure 5. QFN Package with 0.35mm Lead Pitch.

For the wire bonding, ASM Eagle60 wire bonder was used. This wire bonding machine is already capable in bonding fine pad pitch and is already capable of bonding the 60 microns bond pad opening with 70 microns bond pad pitch.

There were two wire bonding techniques used in the evaluation:

1. Forward Bonding
2. BSOB Bonding

The process flow chart for forward bonding is shown in Figure 6 and that of the BSOB bonding is shown in Figure 7. And there were also two lead frame designs being evaluated:

1. Lead frame with 0.20mm thickness (thicker) and a height-to-width ratio equal to 0.20/0.15 (or 1.33)
2. Lead frame with 0.125mm thickness (thinner) and a height-to-width ratio equal to 0.125/0.15 (or 0.833)

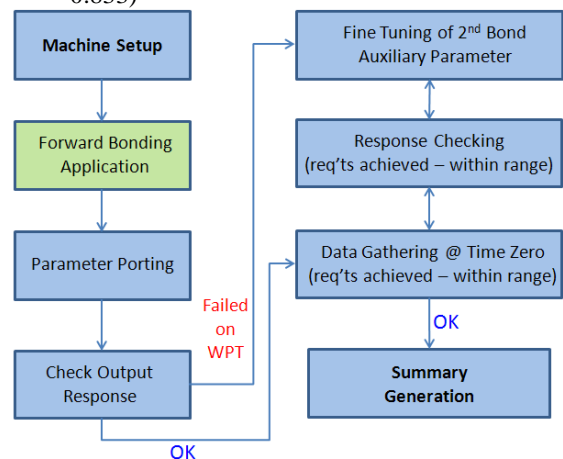


Figure 6. Flow Chart for the Forward Bonding Evaluation.

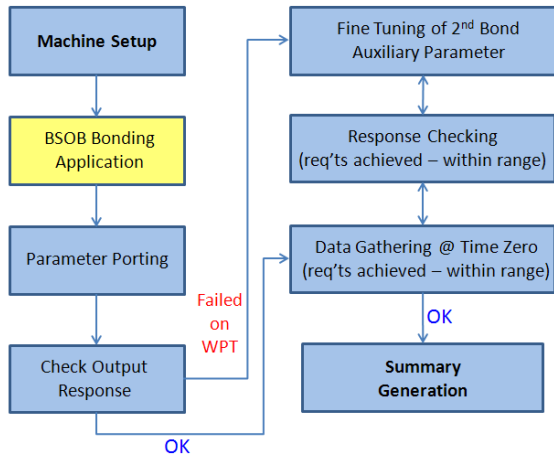


Figure 7. Flow Chart for the Forward Bonding Evaluation.

### 3.2 Modeling and Simulation

To assess the BLR performance of the QFN package, an FEA quarter model was created as shown in Figure 8. This was constructed based on the design shown in Figure 5. A volume-averaged technique was implemented to get the accumulated creep strain energy density per cycle ( $\bar{W}_{cr}$ ) for the bottom interface layer (solder/PCB interface) as well as the top layer (device/solder interface). The fatigue solder life was then calculated using the correlation model for SAC solders. The lower of the two was considered as the solder life.

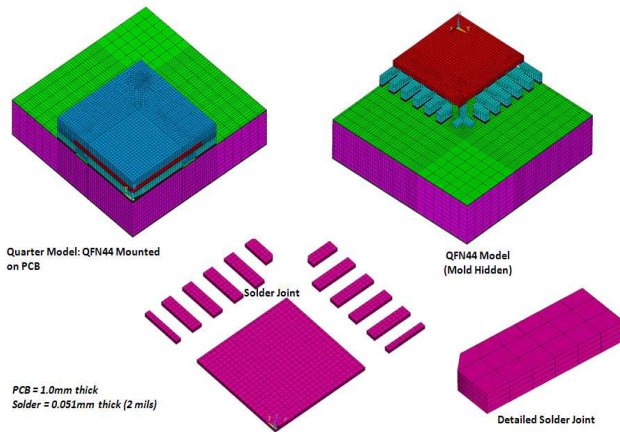


Figure 8. FEA Quarter Model for BLR Simulation.

## 4.0 RESULTS AND DISCUSSION

For the wire bonding evaluation, the first experiment using forward bonding on the thicker lead frame design (height-to-width ratio = 1.33) was not successful. There was a real

issue on bonding wire to the 8 corner leads due to instability.

On the thinner lead frame design (height-to-width ratio = 0.833), forward wire bonding application was still with issues on the corner leads but was better than the result on the thicker lead-frame. It indicates that the lower the height-to-width ratio, the more stable is the lead for wire bonding application. Upon checking the output responses, wire pull test results failed on the corner package leads leading to lifted stitch break mode during wire pull test. Figure 9 shows the wire pull break mode. The difference between a good bond (no fish tail) and the one with a fish tail is illustrated in Figure 10.

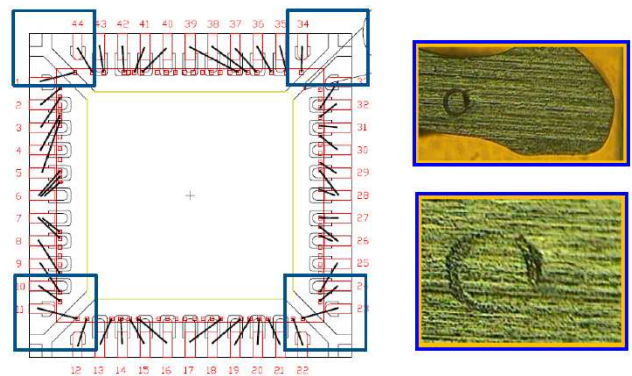


Figure 9. Photo of a Corner Lead with Lifted Stitch.

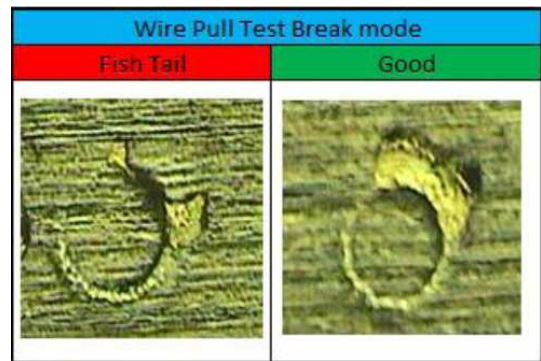


Figure 10. Photo of a Fish Tail and a Good Bond

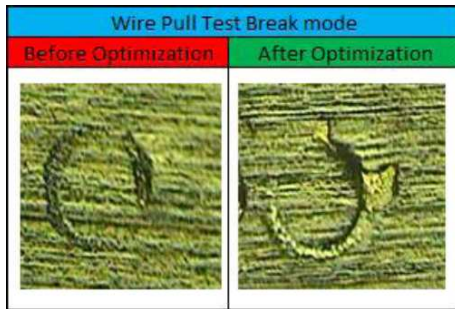


Figure 11. Photo of the Corner Lead after 2<sup>nd</sup> Bond Optimization

After the looping optimization to have good landing area for second bond and the second bond auxiliary parameter optimization to cater to the instability on corner leads, the wire pull response improved (see Figures 12 and 13). There was good stitch formation but there was still intermittent lifted stitch response on wire pull break mode and frequent assist issues such as short tail (see Figure 11).

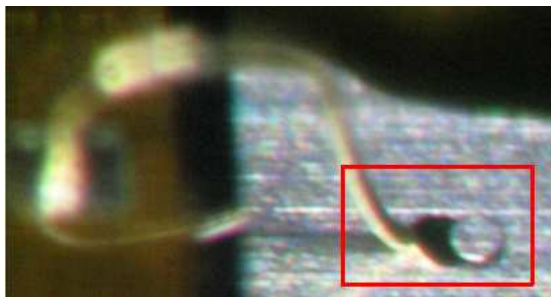


Figure 12. Enhanced Looping to have good landing on 2<sup>nd</sup> bond

With optimized looping and 2<sup>nd</sup> bond auxiliary parameter

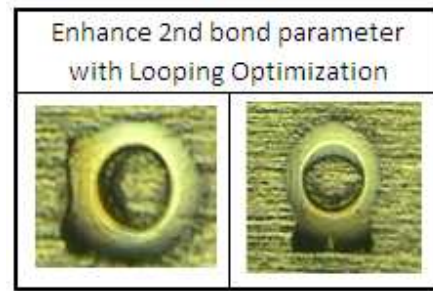
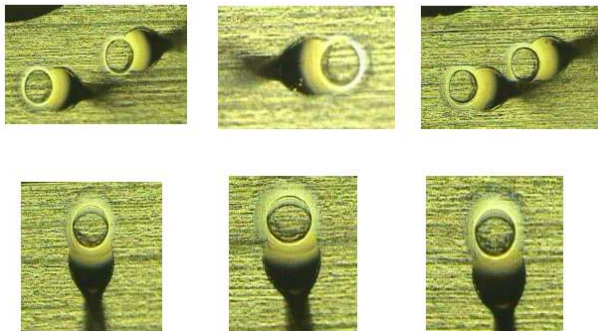


Figure 13. Results of Optimized Looping and Parameters

Based on the forward bonding results, wire pull readings improved through the application of auxiliary parameters and looping optimization but wire pull break mode still needs further improvement.

BSOB wire bonding application was the second trail for this evaluation. The response on 2<sup>nd</sup> bond was good and the inconsistent wire pull break mode on corner leads was being catered by this application. Figure 14 shows that 0.35mm lead pitch QFN package meets wire bond requirements such as wire pull test using BSOB wire bond application.

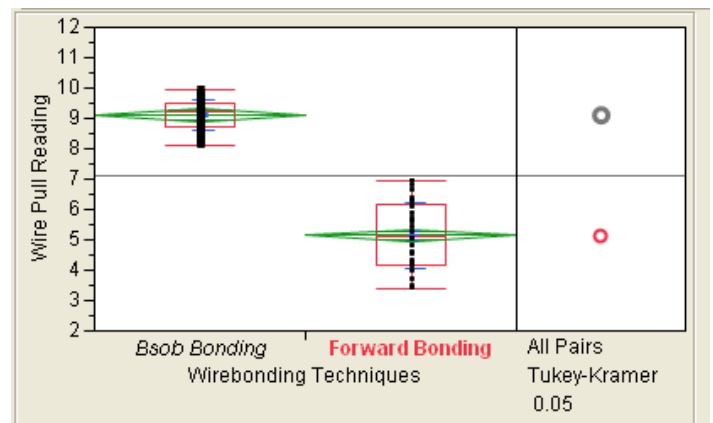


Figure 14. Results of wire pull test on BSOB Wire Bond application.

Above result shows (thru one way analysis of variance) that BSOB wirebond application have significant impact in wire pull test and also key improvement on 2<sup>nd</sup> bond bond issues encountered on this package. Instability issue on corner leads leading to lifted stitch during wire pull was being resolved.

Table 2. Summary of Wire Bond Evaluation Results

Wire Bond Application	Wire Pull Response	Remarks
Forward Bonding (thicker lead frame)	* Second bond was not successful; NSOL (non-stick on lead) encountered	Failed to meet wire bond requirement.
Forward Bonding (thinner lead frame)	* Second bond response was good stitch formation * Intermittent lifted stitch on wire pull break mode response on corner leads	Failed to meet wire bond requirement and observed frequent assists such as short tail
BSOB Bonding (thinner lead frame)	* Instability issue on corner leads resolved * Wire pull break mode meets wire bond criteria	Passed wire bond criteria and with minimal assist during production run

On the board level reliability (BLR) performance assessment, result of the BLR simulation after 3 thermal cycles (2 cycles per hour; 125°C to -40°C) is shown in Figure 15. The critical solder joint is located at the package corner. This joint is expected to fail earlier than the other joints. This critical joint was used for solder life prediction.

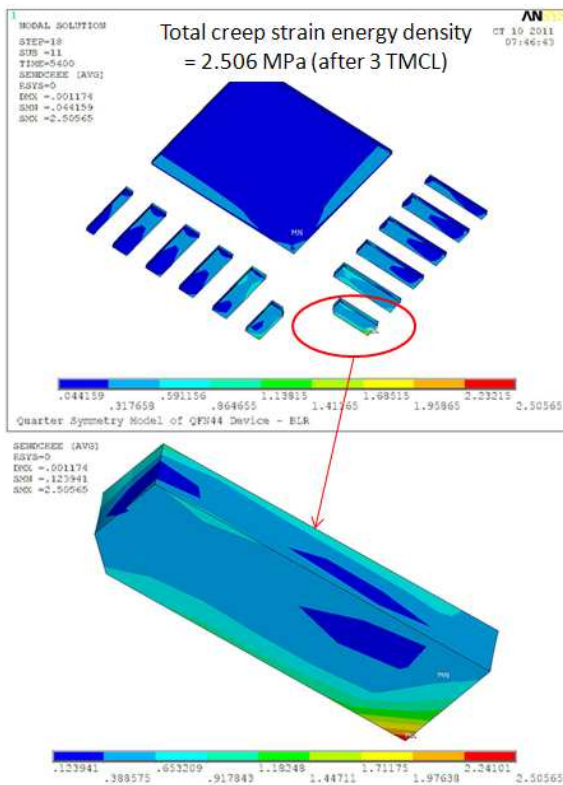


Figure 15. Strain Energy Density Result

The predicted solder life in terms of number of cycles is shown in Table 3. The predicted solder life is 1950 cycles and indicates a good BLR performance. So it means that even with the reduced lead width, the solder or board level reliability is still good. The presence of the center die pad has contributed to a stronger solder connection of the package to the PCB.

Table 3. FEA Solder Life Prediction

Solder Interface Layer	Strain Energy Density (MPa) Accumulated per Cycle	Life Prediction (Cycles)
Bottom Layer (PCB Side)	0.183	1950
Top Layer (Device Side)	0.164	2181

### 5.0 CONCLUSION

From this study, it can be concluded that though QFN package fine pitch technology specifically the 0.35mm pitch has many challenges, successful package development could be achieved by design, virtual prototyping or modeling and wire bonding process optimization.

In terms of wire bonding, BSOB technique results in a more stable and reliable wire-to-leads bonding and better pad/lead stability compared to the standard forward bonding process. It was also shown that lower height-to-width ratio ( $< 1$ ) would provide better lead stability.

Virtual prototyping or modeling provides a fast and cost-effective method of assessing board level reliability (BLR) of a QFN package. The presence of a center die pad would be able to maintain a stronger soldering connection to the PCB and would compensate the reduced lead width or peripheral solder area.

### 6.0 RECOMMENDATIONS

Based on the results, it is highly recommended to use BSOB wire bonding technique for 0.35 mm lead pitch QFN packages when forward bonding is not successful. The lead height-to-width aspect ratio must be considered in order to ensure lead stability during wire bonding. A lead aspect ratio of less than 1 is recommended.

And to ensure a good board reliability (BLR) performance especially for 0.35mm fine lead pitch of the QFN package even before an actual prototype is fabricated, it is also recommended to do virtual prototyping or FEA modeling and simulation.

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### 7.0 ACKNOWLEDGMENT

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