ELIMINATION OF DELAMINATION AND SOLDER FLOW-OUT IN A NEW SYSTEM IN PACKAGE (SIP) WITH LARGE SURFACE MOUNT DEVICE (SMD)

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ABSTRACT

SiP (System in Package) is now becoming very popular as semiconductor industries try to come up with products that offer multiple functions in a single IC package. Capacitors, resistors or other electronic components are combined in a single molded package. But as different components are brought together, there are several challenges that have to be overcome in terms of package design and assembly.

This paper specifically considers the challenges encountered in the development of a new SiP that incorporates large SMD (surface mount device) component. The component is a SMD crystal with formed leads. Due to its size, which is quite large compared to the common SMD component assembled in a molded SiP and the lead free solder and reflow requirements, issues on SMD delamination and solder flow-out were very challenging. So an understanding of the factors involved and the design optimization approach used to ultimately produce a successful SiP with large SMD and free of any delamination or solder flow-out issue would be presented.

1.0 INTRODUCTION

The desire to combine several electronic components into a single molded IC package to get multiple desired functions has led to the development of SiP (System in Package). Instead of separately mounting some electronic components like resistors or capacitors to the PCB (Printed Circuit Board), they are now incorporated into a single package.

In this paper, a new SiP with large SMD (surface mount device) component is considered. Figure 1 shows the schematic of the IC package (SiP) which is primarily composed of a substrate, silicon die and a large SMD crystal with formed leads (Figure 2). The SMD component is mounted to the substrate using lead free solder paste. The size of the SMD is about 6.7x1.4x1.5mm and this has to fit in a 7x8x1.9mm molded package.

However, actual evaluation of the first version of the SiP showed that there were issues of delamination and SMD solder flow-out. Solder voids were also observed at the SMD solder joint. It was noted that this was the first SiP design at [redacted] that had a large SMD in a limited package footprint. In order to resolve the issues encountered, factors involved in the delamination and solder flow-out were investigated and package design optimization focusing on substrate and SMD pad improvement was carried out.

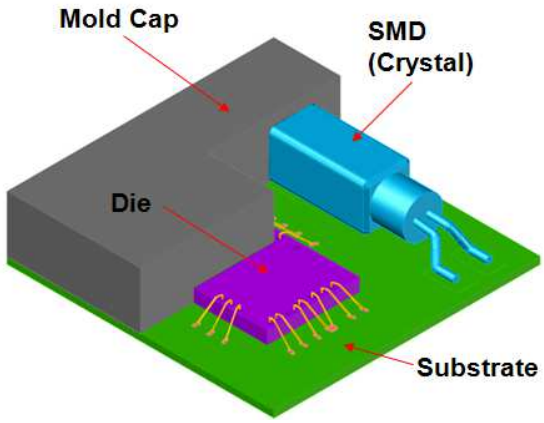


Figure 1. Schematic of a SiP with a large SMD.

Figure 2. SMD Crystal with formed leads.

2.0 REVIEW OF RELATED LITERATURE

2.1 SiP (System in Package)

A System-In-Package (SiP) is a package that combines all of the electronic components needed to provide a system or subsystem in one package, essentially an alternative to a System-On-Chip (SoC). SiPs found their applications in numerous domains and result in a large variety of structures. Digital camcorders have been one of the first adopters of new and innovative packaging technologies. A variety of SiPs are also increasingly found in the RF, digital baseband, transceiver sections of mobile phones and set top box applications that include source decoder, tuner, and channel decoder in the same package. SiP applications also include medical electronics such as smart pills and implanted devices, defense electronics, and aerospace applications [1].

2.2 Lead Free Solder Reflow

2.2.1 Lead-free Solder Void Evolution

Lead-free solders are commonly used in SiPs. However, solder void formation is a very common problem. A study by Li et al [2] provided explanation and a clear understanding of the solder void evolution. Voids in solder joints are formed by the entrapment of gas bubbles during the reflow process. The formation of voids is known to be affected by many process variables including reflow temperature profile, material properties of the flux, and the geometry and solder pattern of the packages.

Figure 3 shows the growth of multiple voids after each subsequent reflow as observed using 2-D X-ray. Tracking of the voids has also proven that voids increase in size when subjected to multiple reflows. Coalescence between the voids may happen during reflow.

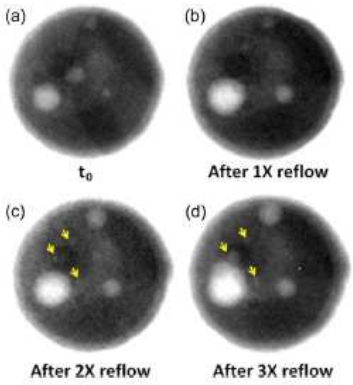


Figure 3. Growth of multiple voids after successive reflows[2]

Another phenomenon called "popping" was also observed when voids migrated to the edge of the solder joints and escape. Figure 4 shows actual observation of how voids grow and migrate to the edge.

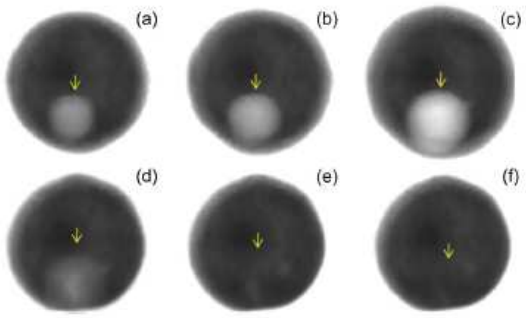


Figure 4. Popping of a solder void [2].

Another study[3] has also collected data showing that multiple reflows always increase the voids.

2.2.2 Moisture Induced Failure During Reflow

With the presence of voids and moisture absorbed in an IC package, moisture induced failure like "popcorn" cracking could happen. Popcorn failure is caused by the damaging effects of moisture when the package is heated to reflow temperature resulting in steam and build-up of vapor pressure. If the hygrothermal stresses and vapor pressure exceed the adhesion strength and fracture toughness of the molding compound, they become the driving force behind the delamination growth and crack formation. As a result, a crack forms that may propagate laterally outwards. When the crack reaches the package exterior, high pressure water vapor is suddenly released producing an audible popping sound.[4]

2.2.3 Controlling Voiding in Reflow Soldering

Voiding in lead-free solder joints can be caused by materials, processes and designs. And there are several ways to control voiding in reflow soldering. Material-wise, a solder formula with good wetting, low outgassing and proper melting sequence are desirable for low voiding. Design-wise, adequate venting channels are critical. This means avoiding large solder coverage or large area soldering under the SMD joint. While process-wise, a balanced reflow profile with maximal drying of volatile and maximal wetting is desired.[5]

3.0 EXPERIMENTAL SECTION

3.1 Design Iterations and Modeling

The first version of the SiP design created was having a larger solder pad or soldering area. The pad was as large as the SMD body (Figure 5). The whole SMD metal body was soldered to the substrate using lead-free solder in a reflow soldering process.

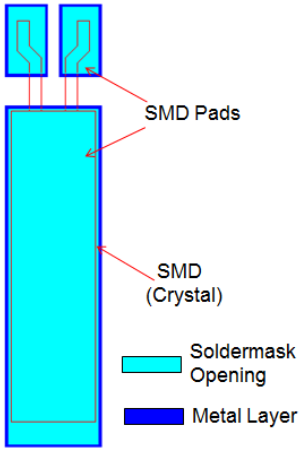


Figure 5. SiP Design (1st version with larger pad)

The designs was also assessed using mechanical modeling to check for warpage and possible issues related to CTE (coefficient of thermal expansion) mismatch. Figure 6 shows the 2D model used in the mechanical modeling and simulation.

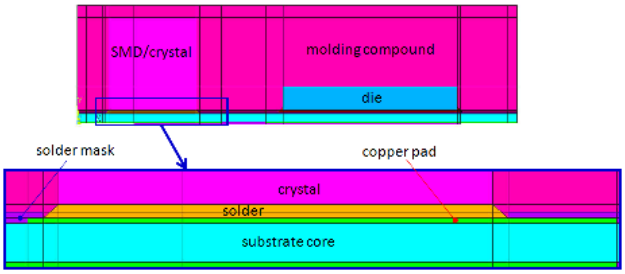
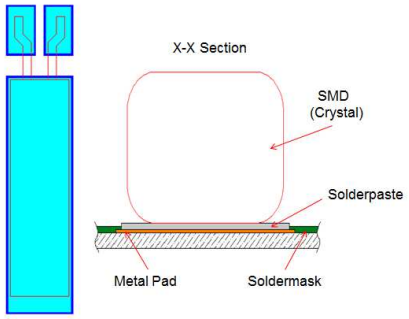
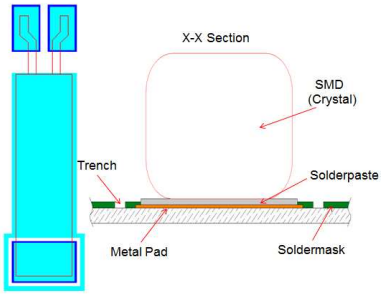
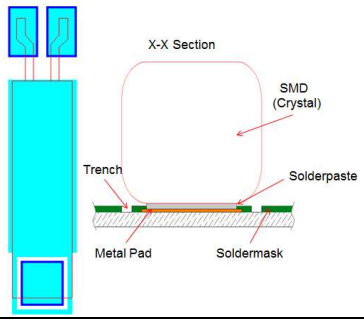


Figure 6. SiP 2D model

Then design iterations were done to come up with another improved versions as summarized in Table 1. The focus was on optimizing the substrate design. For design iterations 2 and 3, pad size was reduced and substrate trench was added to improve package performance against delamination and solder flow-out. But design iteration 3 has the smallest solder pad among the 3 SiP designs considered.

Table 1. SiP Design Iterations

Design #	Illustration	Changes Made
1		1st Version (SMD Pad length as long as crystal body)
2		2nd Version (SMD pad length reduced; pad width the same; trench added)
3		3rd / Final Version (SMD Pad width further reduced; trench added)

3.2 Moisture Sensitivity Level (MSL) Evaluation

The different SiP design versions were then evaluated by subjecting the units to MSL 3 test (192 hours at 30°C/ 60% RH) after assembly. This means that the lead-free solder for the SMD would be subjected to multiple reflows (4 cycles); one cycle (1x) during surface mount and three cycles (3x) during MSL reflow at 260°C. There were two solder types used in the mounting of SMD to the substrate. Lead-free solder 1 is the standard solder used and lead-free solder 2 is the alternative solder, which has a higher melting temperature than solder 1.

Packages were then checked for solder flow-out after MSL reflow. Visual inspection, SCAT and cross-section analysis were performed to verify solder flow-out and delamination. Thermal cycling was also conducted to ensure that the package would be free from solder reliability issue and no

crack propagation. Table 2 shows the evaluation matrix being considered in the study.

Table 2. SiP Evaluation Matrix

Leg #	Substrate Design	Solder Paste Material
1	Design #1	Lead-free Solder 1
2	Design #1	Lead-free Solder 2
3	Design #2	Lead-free Solder 1
4	Design #2	Lead-free Solder 2
5	Design #3 (Final Version)	Lead-free Solder 1
6	Design #3 (Final Version)	Lead-free Solder 2

4.0 RESULTS AND DISCUSSION

Results based on package mechanical modeling show that warpage is relatively low (Figure 7). Actual package observation also confirmed the predicted low package warpage. Interface stress due to CTE (coefficient of thermal expansion) mismatch is also relatively low, which implies that delamination is not primarily due difference in CTE of the materials at MSL reflow temperature but other factors are involved that triggers mold-substrate delamination initiating at the SMD solder edge.

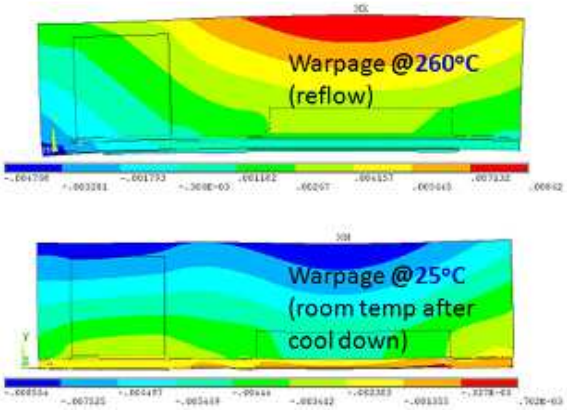


Figure 7. Package warpage at MSL reflow and room temperature.

After evaluation of the first design version using the standard lead-free solder material (lead-free solder 1), SCAT and visual inspection showed delamination and solder flow-out (Figure 8). A lump of solder material was seen after MSL reflow on the side of the package with external micro-crack due to "popcorn" effect. Cross-section results confirmed the observed delamination as shown in Figure 9. Solder voids were also observed with X-ray and cross-section. The big gap or void seen at the edge of the solder seems to be due to some solder voids that combines with other voids and migrated to the edge and then some space left during solder flow-out along the delaminated surface.

It is believed that migration of solder voids to the solder edge of the SMD as also discussed in a related study [2] creates high stress concentration at that location as the entrapped gas within the void builds up high pressure at high temperature reflow condition. This would be further aggravated by moisture absorbed during MSL soak that would turn into steam with high pressure. This supports observation of delamination that initiated at the SMD solder edge and propagated along the mold-substrate interface. At high temperature (260°C MSL reflow), the solder is in molten state and would be pushed or flow along the delaminated mold-substrate interface.

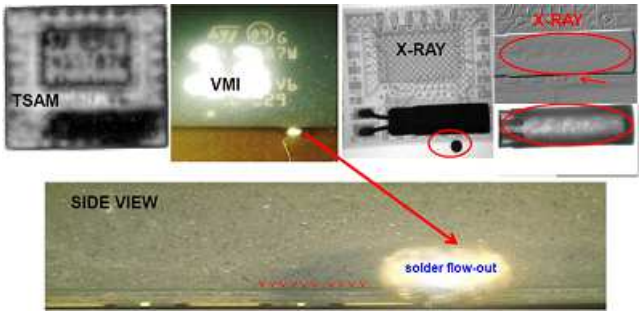


Figure 8. SCAT/visual inspection results of the larger pad design (1st version with lead-free solder 1).

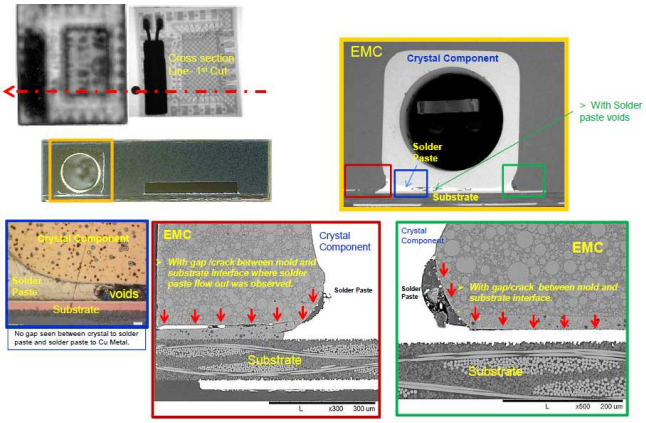


Figure 9. Cross-section results of the larger pad design (1st version with lead-free solder 1).

Further analysis by mechanical decapsulation of the evaluated units also revealed footprints or traces of large solder voids all over the bottom of the SMD as well as solder flow-out. Figure 10 shows the results of decapsulation of the new SiP developed with large SMD.

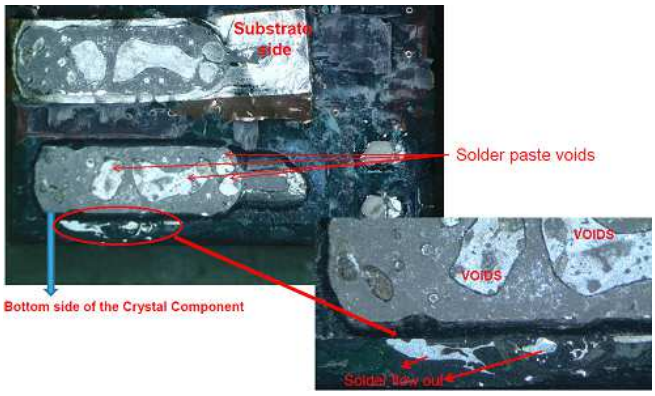


Figure 10. Mechanical decapsulation results (Evaluation Leg #1).

For the 2nd evaluation using a solder material with higher melting temperature (Evaluation Leg #2), the 1st design was also having a delamination and solder flow-out problem. Figure 11 shows the SCAT and cross-section results. The delaminaton signature is similar to that of the 1st evaluation (Evaluation Leg #1) in which the delamination initiated at the SMD solder edge. This implies that using an alternative lead-free solder with higher melting temperature would not help eliminate delamination or solder flow-out. The melting temperature of solder 2 was higher but still below the MSL reflow temperature.

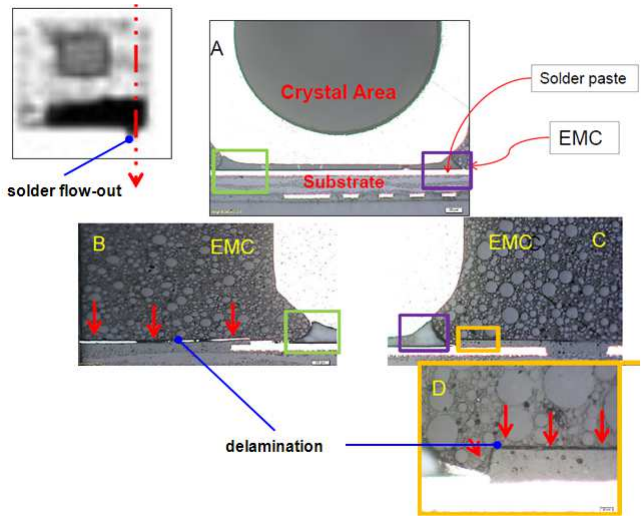


Figure 11. Results of the larger pad design (1st version with lead-free solder 2 – Evaluation Leg #2).

For the 2nd SiP design version (Evaluation Leg #3 and #4), results showed a better performance. Though there were still solder voids observed, mold-substrate delamination and solder flow-out were not encountered. The reduction in pad size (i.e. smaller solder area coverage) lowers the relative percentage of voids and the substrate trench somehow has improved mold-substrate interface adhesion that helps contain molten solder during multiple high temperature reflow cycles. The units also survived 1000 thermal cycles (TC) after the thermal cycling evaluation.

Evaluation results of the final SiP design version with the smallest solder pad (Design #3) are shown in Figure 12 for Leg #5 and Figure 13 for Leg #6. There was no mold-substrate delamination and solder flow-out issue was not encountered. There was also no failure until 1000 thermal cycles. Though some solder voids were seen from cross-section results, no delamination propagated from the solder edge. It could be that due to the lower percentage of voids (smaller solder area) relative to the overall substrate interface area, the pressure build up within the voids was not enough to overcome interface adhesion and initiate delamination.

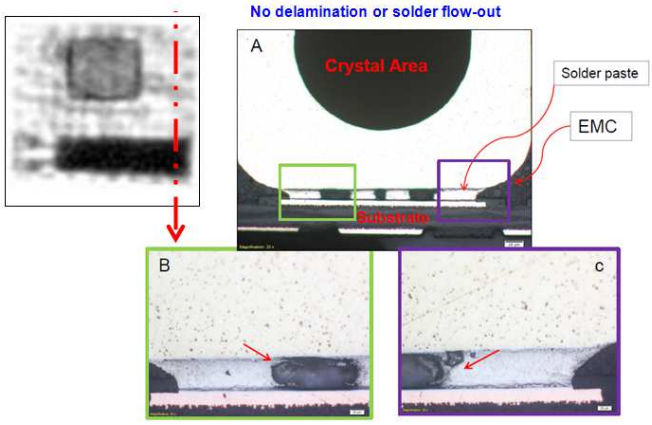


Figure 12. Results of the smallest pad design (final version with lead-free solder 1; Leg #5).

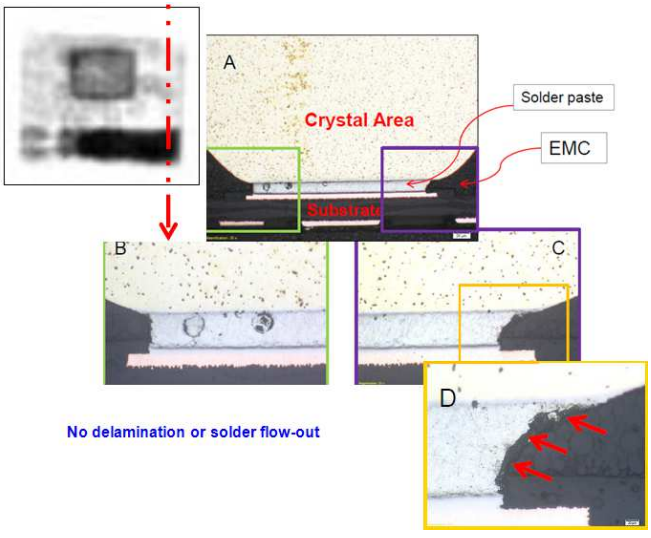


Figure 13. Results of the smallest pad (final version with lead-free solder 2; Leg #6).

Table 3 summarizes the results of the evaluation. Based on the results, the designs with the reduced SMD pad size and substrate trench (Design #2 and Design #3) perform better with no delamination and solder flow-out. Result show that adding a substrate trench around the solder area improves interface adhesion to counter the tendency of the interface to delaminate when subjected to multiple high temperature reflow cycles.

Table 3. Summary of Evaluation Results

Leg #	Results	Remarks
1	Failed	With delamination and solder flow-out at MSL reflow
2	Failed	With delamination and solder flow-out at MSL reflow
3	Passed	No failure until 1000TC
4	Passed	No failure until 1000TC
5	Passed	No failure until 1000TC
6	Passed	No failure until 1000TC

5.0 CONCLUSION

Based on this study, it can be concluded that developing SiP with large SMD in a limited package footprint would be very challenging because of delamination and solder flow-out issues but success could be achieved by understanding the factors involved and optimizing substrate design.

In terms of substrate design, the solder pad must be as small as possible to avoid large solder coverage or large area soldering that is prone to solder voiding resulting in delamination and solder flow-out. Adding a substrate trench also helps improve interface adhesion and lower the risk of delamination and solder flow-out.

A clear understanding of solder void evolution during multiple subsequent reflows and its effect on IC package reliability is necessary to resolve issues in SiP involving lead-free solder. Modeling also provides important information to determine if delamination is not mainly due to CTE mismatch or poor thermo-mechanical performance.

6.0 RECOMMENDATIONS

Based on the results, it is highly recommended to optimize substrate design when developing SiP with large SMD to be assembled or any package that involves large area soldering.

Since this study has focused primarily on substrate design to eliminate delamination and solder flow-out, it is also recommended that process optimization or selection of better solder materials for SiP applications be conducted to control solder voiding problem.

7.0 ACKNOWLEDGMENT

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