ELIMINATION OF VOIDS AND DELAMINATION IN UNBALANCED STACKED DICE BY OPTIMIZING SUBSTRATE DESIGN

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ABSTRACT

Miniaturization is now the trend in semiconductor. Smaller and thinner package is prime objective. Stacked dice process in laminates now becoming very popular as semiconductor industries try to come up with products that offer multiple channels in a small IC package. Digital and analog dice combined in stacked lay-out maintaining thin molded package. But as different dices are brought together, there are several challenges that have to be overcome in terms of package design and assembly.

This paper specifically considers the challenges encountered in the development of a compact and thinner package that incorporates analog and digital functions in one. Digital die is smaller than analog die and must be the first one to be die bonded prior analog die, this makes the internal construction as *unbalanced* stacked dice. Normally, stacked dice is in pyramid lay-out, wherein a single large die supports smaller top die. Success is measured when there is a solution to control voids and eliminate delamination for *unbalanced* stacked dice as mentioned. So an understanding of the factors involved and the design optimization approach used to ultimately produce a successful unbalanced stacked die in a thin package using thin substrate would be presented.

1.0 INTRODUCTION

The desire to combine several dice into a single molded IC package to get multiple desired functions has led to the development of Stacked dice LGA 5X5X0.55. Instead of separately mounting some electronic components like analog ICs and Digital ICs to the PCB (Printed Circuit Board), they are now incorporated into a single package.

In this paper, the internal construction must be designed to stack smaller analog die (2.740X2.093sq mm) at the bottom and larger digital die (3.052X3.032sq mm) on top. (see Figure 1). An interposer silicon die (2.000X 0.900 sq mm) was added as bottom die to support the die overhang of digital die. (see Figure2) These stacked dice will be supported by 0.13mm substrate and be molded with 0.42mm mold cap. External construction is an Ultra thin Fine pitch Land Grid Array 79L; UFLGA79L 5X5X0.55 (LXWXH).

However, actual evaluation of the first version of the UFLGA79L showed that there were issues of delamination between top and bottom dice; and die attach voids between bottom die and substrate. Note that this is the first "non-pyramid" stacked design at ST-Calamba with limited stacked-up and footprint. In order to resolve the issues encountered, factors involved in the delamination and voids were investigated and package design optimization focusing on substrate was carried out.

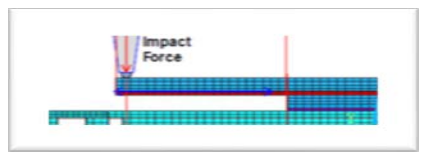
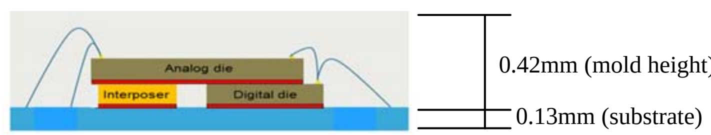


Figure 1. Cross section illustration of unbalanced stacked die (Top die overhang) that will affect wirebonding.



	L (mm)	W (mm)	T (mm)
Top die	3.052	3.032	0.105
Bottom die	2.740	2.093	0.105
Silicon Interposer	2.000	0.900	0.105

Additional Silicon die to support top die

Figure 2. Cross section illustration with Interposer added to support Analog die overhang.

2.0 REVIEW OF RELATED LITERATURE

2.1 Stacked die using DAF on Substrates

Stacked die robust die attach material is the Die Attach Film (DAF). Currently DAF has being widely applied on various high density packages such as CSP, SIP, POP and so on due to its bleedless, consistent bond line thickness (BLT), simple operation Fig.3 shows typical assembly flow of plastic ball array packages (PBGA) with dicing die attach film (DDAF), which die-attach film and dicing tape are integrated inside. Traditional assembly flow with liquid-type die-attach material can be easily applied onto packaging with DAF. Besides, process is simplified by eliminating dispensing and skipping cure post die-attach. However, DAF void always is one of major concerns, especially for its application between die and plastic substrate. Reliability issue of delamination or popcorn likely occurs at the DAF/substrate interface

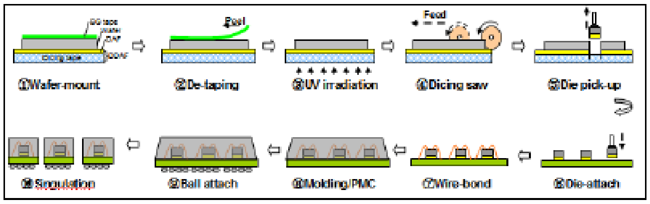


Figure3. General assembly flow with DDAF

DAF void characteristic and its formation/reduction mechanism are studied. Besides die bonding parameters, there should have many factors contributed to void performance. For UFLGA79, DAF voids between bottom dice and substrate were also considered one of the contributors for top die delamination issue.

2.2 Substrate construction and electrical signals.

Substrate is normally constructed with metal planes to ensure Cu balance and solder mask balance between layers that to ensure no substrate delamination when subjected to reflow.

Electrical simulators in relation to the metal plane or metal strips in substrate should govern for Resistance, Self-Inductance and Self-capacitance.

Figure 5 shows the 2 layer (top side – M1 and bottom side-M2) construction of the substrate for UFLGA79, with metal balance of 16%.

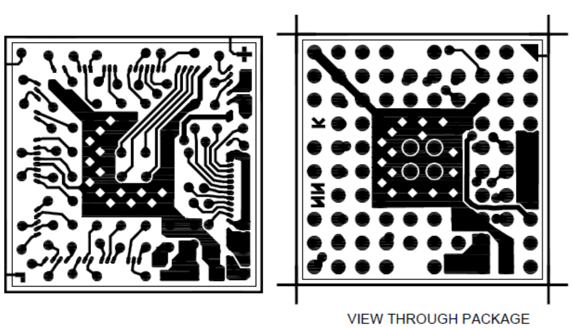


Figure 5. Top side and Bottom side viewed through package.

3.0 EXPERIMENTAL SECTION

3.1 Design Iterations and Modeling

The first version of the UFLGA79 design created was using **rigid and thin** DAF (20um) for all stacked dice to ensure planarity in-between interfaces – 2 bottom dice to substrate and top die to the 2 bottom dice, and to ensure there is enough clearance for the wirebond looping after mold.

Back-end assembly of UFLGA79 performed (Die attach to package singulation) and subject samples for Moisture Sensitivity Level 3 to check for delamination.

Result: Top die delaminated from bottom dice and observed DAF Voids after cross-section validation. See figure6.

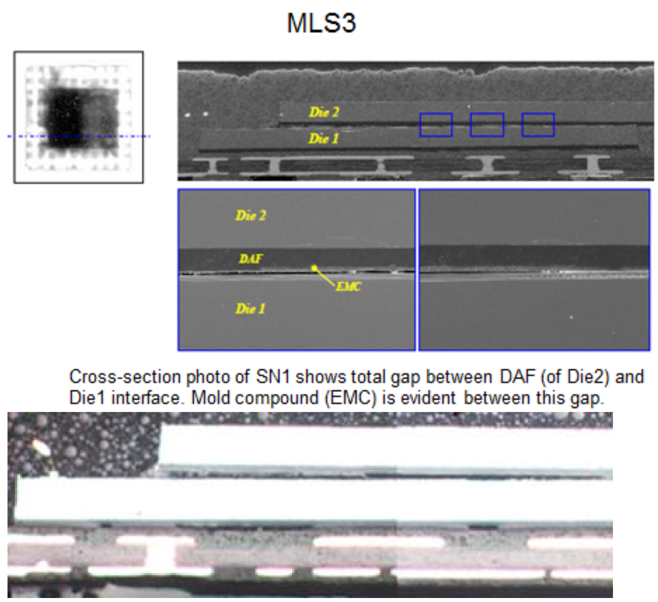
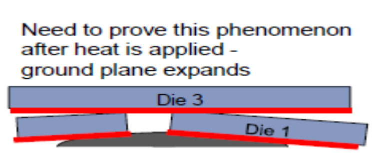


Figure6. Top die delamination and Bottom die voids

Fault- tree analysis performed:



3.2 Correlation between void and substrate topography

Now that void occurs at the substrate/DAF interface with fixed pattern, affecting top die to delaminate, the substrate topography is mostly suspected. Figure 7 shows that to identify the correlation between void and substrate surface, the cross section was further analyzed and found out that the metal plane expansion serves as fulcrum (not only as source of voids) thus affecting the planarity of 2 bottom dice which resulted to top die aggravated delamination. Therefore, the ground metal plane serves as peaks and solder mask as valleys.

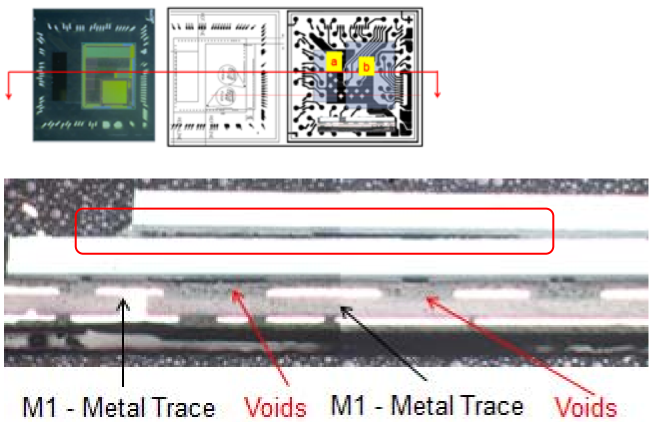


Figure7. Correlated metal trace plane serves as fulcrum and induces void, thus top delamination encountered.

Observe that in every after metal plane, there is large void between die and substrate. Measurements of the peaks and valley were more than 10um, the thickness of DAF is 20um in this work, namely DAF need fill the gap with depth equivalent with 50% of its thickness, which produces the challenge toward DAF gap filling capability. Therefore, these voids result from the insufficient gap and it can be explained that DAF voids have the properties of fixed position and similar pattern, which is matched with substrate surface topography.

A comparison of non-planarized and planarized substrate was performed to check the difference as shown in Figure 8. Difference of more than 5 microns observed.

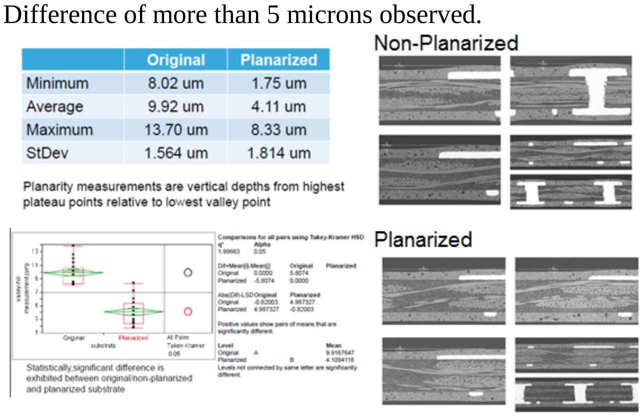


Figure 8. Non-Planarized vs. Planarized.

Design Iterations:

Considering the above findings from Fault tree analysis upto cross section verification, the rootcause of die top delamination and voids between bottom dice and substrate is the substrate topography. Softer and thicker DAF for top die was considered to compensate variation of level of the two (2) bottom dice. Table 1 was considered to further validate the hypothesis using the existing materials in the production line:

Leg #	DAF (Fix)	Substrate (with variation)	Remarks
1	Top die and Bottom dice – rigid and thin (20um)	Non-planarized – existing for UFLGA79	Control Leg, Samples should fail MSL3 to validate the issue (with cross section validation).
2	Top die – softer and Thicker DAF (30um), Bottom dice – rigid and thin (20um)	Non-planarized – existing for UFLGA79	Samples must pass MSL3 with cross section validation.
3	Top die – softer and Thicker DAF (30um), Bottom dice – rigid and thin (20um)	Planarized from other package	Response in time (0) with cross-section validation.

Table1: Evaluation matrix

4.0 RESULTS AND DISCUSSION

Results based on package Thermo-mechanical modeling (TMM) showed that warpage is relatively low (Figure 9). Actual package observation also confirmed the predicted low package warpage. Interface stress due to CTE mismatch is also low which implies that delamination could be due to other factors.

Result of TMM showed low risk if DAF material adhesion is high.

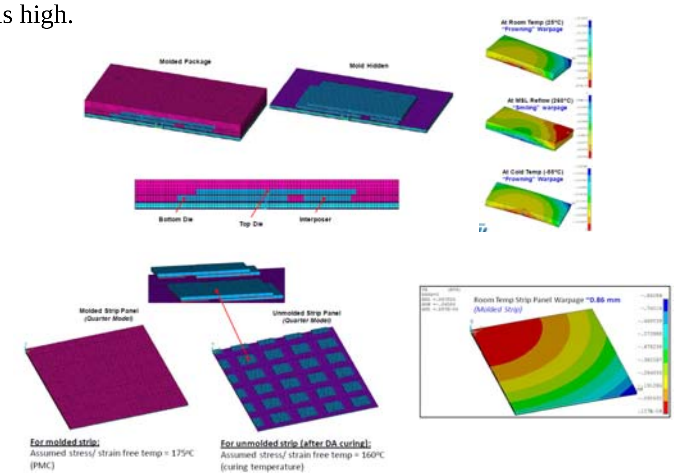


Figure9. UFLGA79 Thermo-mechanical simulations - package level and strip level.

Results:

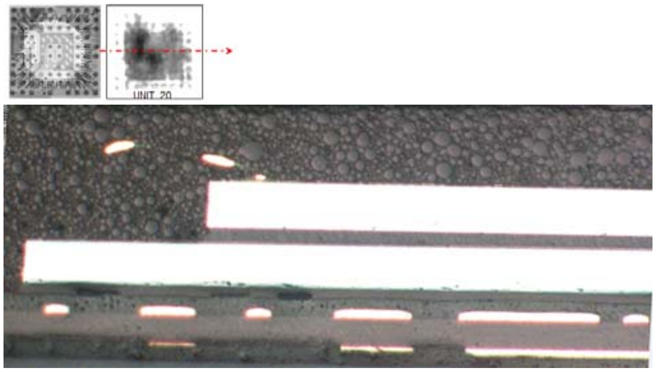


Figure10. Back-end assembly was performed using Softer and Thicker DAF for top die passed MSL3.

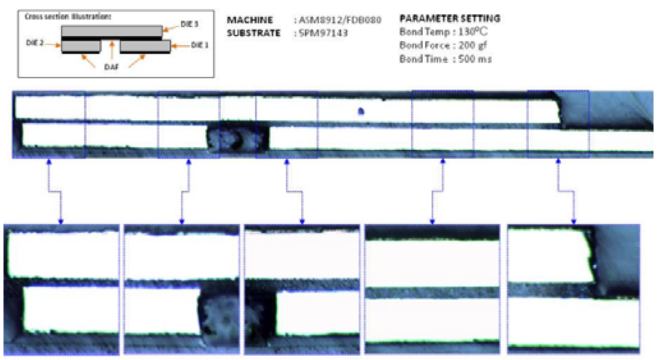


Figure11. Die attach stacked die using same rigid and thin DAF showed zero (0) voids for bottom dice at time (0).

Table 3 summarizes the results of the evaluation. Based on the results, top die should use softer/ thicker DAF while bottom dice should use Rigid and Thinner DAF on a planarized substrate.

Table3. Summary of Evaluation Results

Leg #	Results	Remarks
1	Fail	Previous Issue replicated
2	Pass	Passed MSL3
3	Pass	Passed Die Attached responses

5.0 CONCLUSION

Based on this study, it can be concluded from the summary results, planarized substrate should be considered for DAF application. Top die to use softer/ thicker DAF to compensate variation of bottom dice, while bottom dice should use Rigid and Thinner DAF to maintain level.

New Substrate Design for UFLGA 5X5X0.55 79L proposal is shown in Figure10, replacing the metal plane in M1 with strip type metals and reducing M2 density resulted to better Cu bance.

Note: Figure 11 to 13 shows no significant difference in Electrical modeling well for Resistance, Self-Inductance and Self-capacitance.

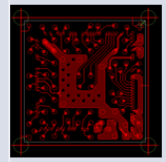
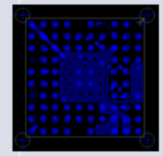
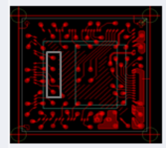
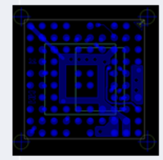
2 layer, 0.13mm	M1: Layer 1	M2: Layer 2	Cu Balance
Original Design			16%
New Design (Cu Metal Plane change to metal strips)			6% (better)

Figure12. Proposed planarized substrate from metal plane to metal strips M1: layer 1

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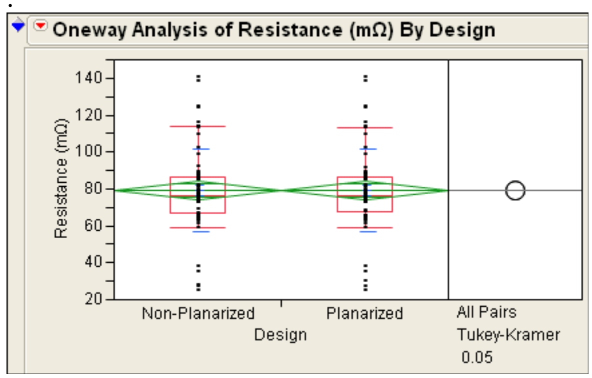

Figure13. No significant difference in resistances of all nets (signal traces + bondwires) between the two designs – Non-Planarized and Planarized.

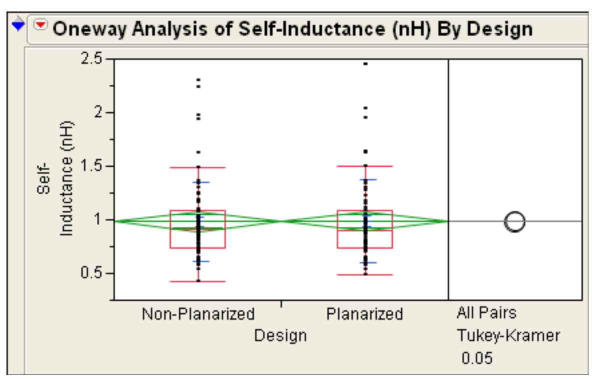

Figure14. No significant difference in self-inductances of all nets (signal traces + bondwires) between the two designs – Non-Planarized and Planarized.

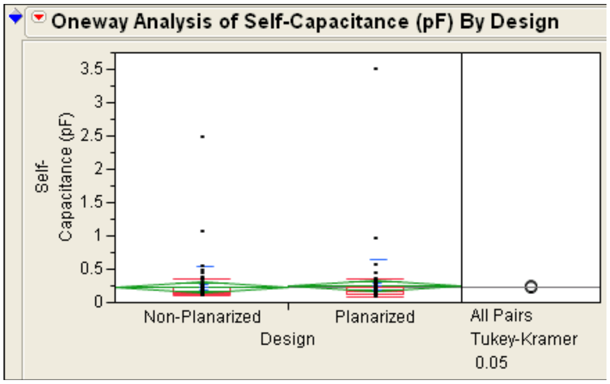

Figure15. No significant difference in self-capacitances of all nets (signal traces + bondwires) between the two designs – Non-Planarized and Planarized.

6.0 RECOMMENDATIONS

Based on the results, it is highly recommended to optimize DAF selection and substrate design when developing stacked die.

Since this study has just focused on substrate design to eliminate delamination and voids, it is also recommended that DAF selection should be considered to ensure robustness of material selection.

7.0 ACKNOWLEDGMENT

The authors would like to thank the Corporate Package & Automation members of STMicroelectronics Calamba who were involved in the UFLGA79 package development especially Frederick Arellano and Mark Julius Mapula for die attach various evaluations, and Janet Jucar for the reliability and failure analysis data included in this study.
Jefferson Talledo supported well in the Thermo-mechanical simulations and DAF material recommendations.

8.0 REFERENCES

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